

How to Verify MIPI Conformance Using the J-BERT M8020A High-Performance BERT

Overview

The wide spread and rapid development of cell phones from simple voice-capable devices to smart phones or even tablet PCs with the constant addition of capabilities and features came along with a proliferation of interfaces between ASICs and “sensors” and “terminal devices” such as microphones, cameras, loudspeakers, displays, and peripheral electrical devices as depicted in Figure 1a, which made ASIC development and system integration an increasingly difficult task.

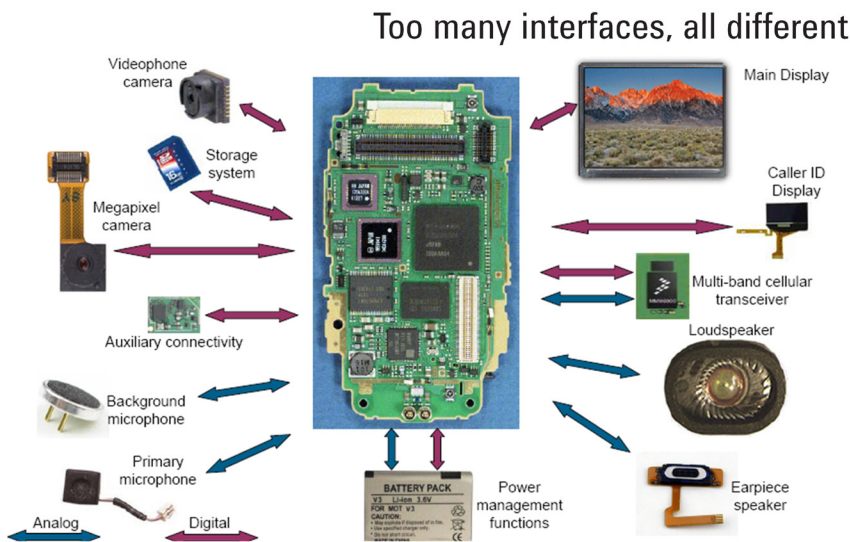


Figure 1a. Smartphone with a variety of interfaces to sensors, terminal, and electrical peripheral devices.

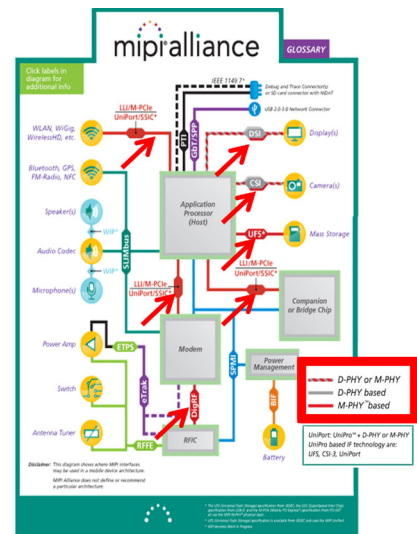


Figure 1b. Block diagram and the use of buses standardized through the MIPI alliance.

The MIPI organization was founded in 2003 (MIPI standing for Mobile Industry Processor Interface) in order to structure the intestines of “mobile devices ranging from smart phones, wireless-enabled tablets and netbooks” and to “benefit the entire mobile industry by establishing standards for hardware and software interfaces in these devices” enabling reuse and compatibility in mobile devices making “system integration less burdensome than in the past.” “The distinctive requirements of mobile terminals drive the development of MIPI Specifications.”¹

In Figure 1b the high speed interfaces are marked with red arrows. By not defining these interfaces as monolithic blocks (such as it is done in computer standards e.g. USB or PCIe) but instead separating the Phy- from the protocol-layer, it was possible to address the variety of sensors and terminal devices with only two different high speed Phy-layers.

Figure 2 shows the different MIPI-standards, which protocols reside on D-PHY and M-PHY respectively, which application they serve, and which kind of test equipment is used for either protocol verification or validation of Phy-layer interoperability/conformance to specifications.

1. <http://mipi.org/momentum>

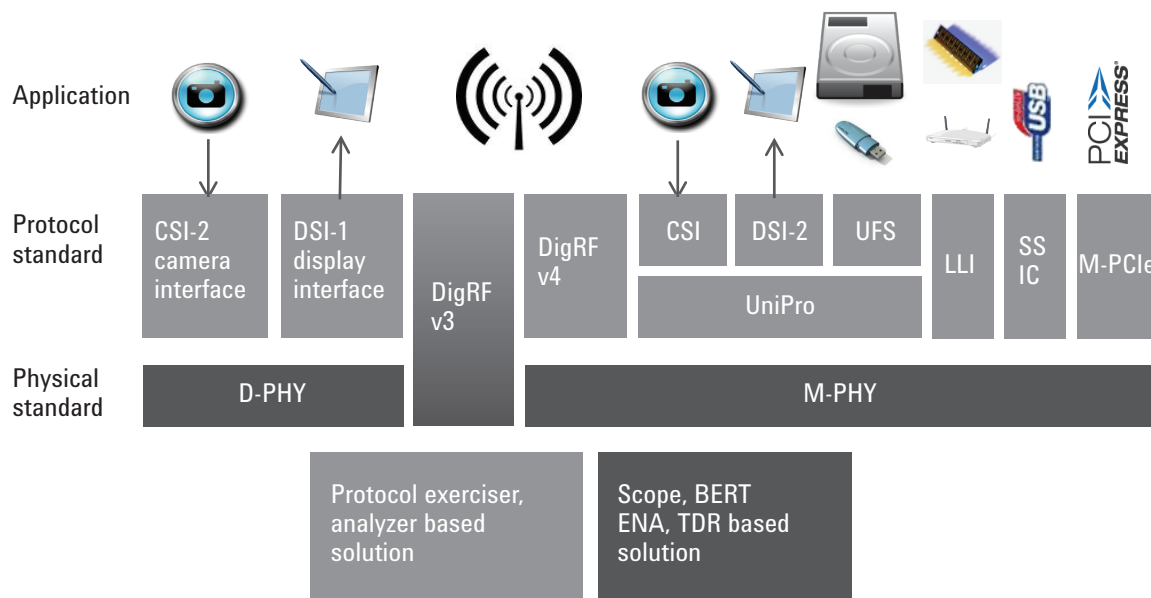


Figure 2. Structure of MIPI high-speed digital standards with separate protocol- and Phy-layer

In M-PHY, for high speed transmission, 4 speed classes (so-called gears) have been defined/ projected with two slightly different rates per gear. Starting at 1.248 or 1.458 Gb/s for Gear 1A or 1B respectively the data rates doubles from one gear to the next reaching to the 10 Gb/s range with Gear 4. As a link can consist of a multitude of lanes, with data being striped across the lanes, even higher aggregate BW can be achieved.

What needs to be tested?

MIPI does not run a compliance program because the specified interfaces are not user accessible (other than for the above mentioned computer standards). Nevertheless, semiconductor vendors and system integrators are interested in validating spec conformance of ASICs and modules in order to verify interoperability and by this allow flexibility in design and selection of parts and vendors.

The sheer amount of tests specified in the CTS (Conformance Test Suite) requires automation for in-situ calibration and test, which Keysight Technologies, Inc. delivers with its N5990A option 165, available for all BERTs, i.e., the heritage models as well as the new J-BERT M8020.

Throughout the remainder of this document we will now focus on one important aspect of testing according to the M-PHY standard, i.e., the high-speed receiver (HS_RX) jitter tolerance test. The definition and the very complex jitter cocktail required for M-PHY high speed receiver (M_HS_RX) test is visualized in Figure 5 (for details see application note Keysight Publication number 5991-2848EN).

Random Jitter RJ(pp)=TJ-DJ is calculated

$$RJ_{RX} = TJ_{RX} - DJ_{RX} = 0.17UI = \sqrt{STRJ^2 + MTRJ^2} = \sqrt{0.1^2 + 0.14^2}$$

$$STRJ_{RX} = STTJ_{RX} - STDJ_{RX} = 0.1UI \text{ (with } STDJ_{RX} = DDJ_{RX} + STSJ_{RX})$$

Receiver has the same RJ budget as Transmitter

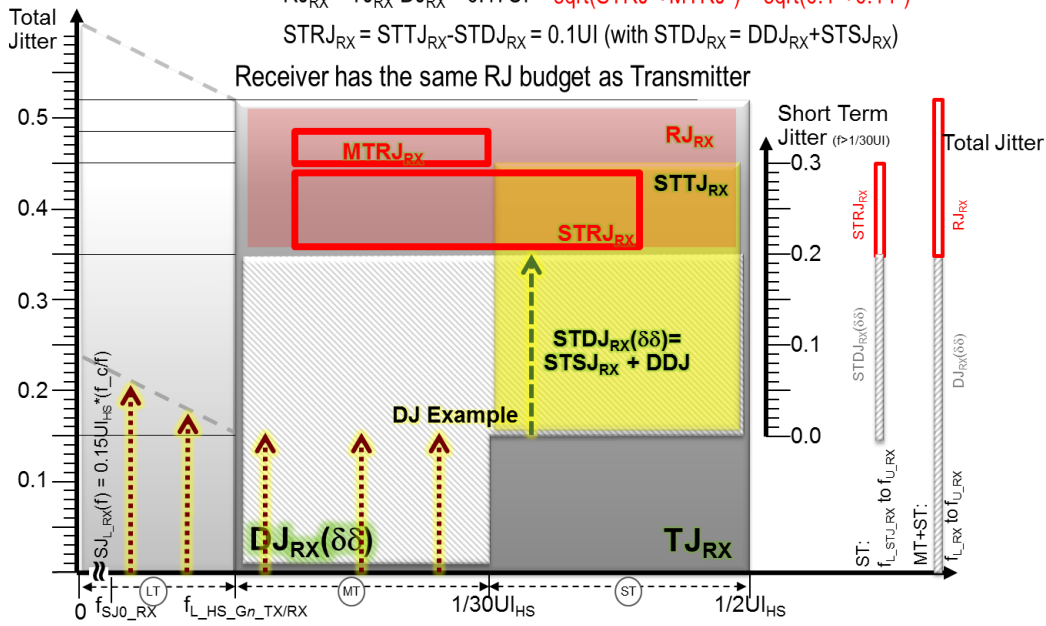


Figure 3. Jitter "cocktail" for M_HS_RX test.

Step	Action	J-BERT parameter	Target value	Pattern	TIE-HP-filter
1	Adjust wideband RJ (>f _{L_RX}) to achieve STRJ	RJ	0.10 UI _{pp} 7.9 mUI _{rms}	clk/2 (1010)	1/30 UI
2	Add low frequency RJ (<1/30 UI) to achieve RJ=TJ-DJ	BUJ	0.17 UI _{pp} 13.5 mUI _{rms}	clk/2 (1010)	f _{L_RX}
3	Turn all RJ off; calibrate SJ (f _{SJ1} , f _{SJ2} , f _{SJ3} , f _{SJ4})	PJ1	0.15 UI _{pp}	CJPat	Off
4	Turn all SJ (and RJ) off; calibrate STSJ (240 MHz) to achieve STDJ (STSJ=STDJ-DDJ)	PJ2	0.2 UI _{pp}	CJPat	Off

Table 1. Steps to achieve proper calibration of jitter for RX testing (numbers refer to M-PHY CTS rev. 1.0).

Jitter tolerance same as most other tests are performed on a single channel. However, for multilane realizations additional skew tests for TXs as well as for RXs are required. J-BERT M8020 being configurable for multiple lanes will provide synchronous start of patterns with individual skew per lane with a future SW release, and by this will as well master this task as it is e.g. demanded for LLI (see Figure 2).

Conclusion

As shown above, the requirements for testing ASICs according to the MIPI specification and CTS are perfectly matched by the J-BERT M8020A: Its high integration allows the test setup to be simple despite the required complex jitter cocktail and its test automation makes in-situ calibration and testing an easy task.

Furthermore, M8020A with its modularity provides the flexibility to adapt to test needs and budget. For example, different speed options can be selected, depending on the speed class to be addressed. The M8041A can also be configured as a single or dual channel module and an additional M8051A module can be added, depending on the number of lanes to be tested. They can also be configured as a generator only (omitting the ED), when the DUT shall not be tested in loopback mode or doesn't support it.

Further details about features and specifications can be found in the data sheet.

Publication title	Publication number
<i>J-BERT M8020A High-Performance BERT</i> – Data sheet	5991-3647EN
<i>M8048A ISI Channel</i> – Data sheet	5991-3648EN
<i>M9052A and M9505A 2-and 5 Slot AXIe Chassis</i> – Data sheet	5990-6584EN

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